

The diagram illustrates a multi-channel UTOPIA receiver system. It features two parallel input channels, each starting with an S/P (Serial-to-Parallel) converter (40) receiving RXCK, RXSYNC, and DSTi signals. The outputs of these converters feed into Cell Delimiters (42). A dashed line separates the two channels, indicating parallel processing. Each channel's output from the Cell Delimiter goes to an ICP Processor (44), which then feeds into an IMA Frame State Machine (46). The outputs of the IMA Frame State Machines feed into a central RAM Controller (48). The RAM Controller is connected to a RAM Area (56) and an RX Scheduler (60). The RX Scheduler outputs to a UTOPIA Interface (62). The RAM Controller also feeds into a Rate Recovery block (58). The Rate Recovery block outputs a Recovered Cell CLK signal to the RX Scheduler. The Cell Delimiters (42) also feed into Link Info Registers (50) and an ICP Cell With Changes Buffer (52). The Link Info Registers (50) feed into a PCM Ring Control block (33). The ICP Cell With Changes Buffer (52) feeds into a Microcontroller (54). The PCM Ring Control block (33) and the Microcontroller (54) are connected to a common bus (54).

## Figure 2

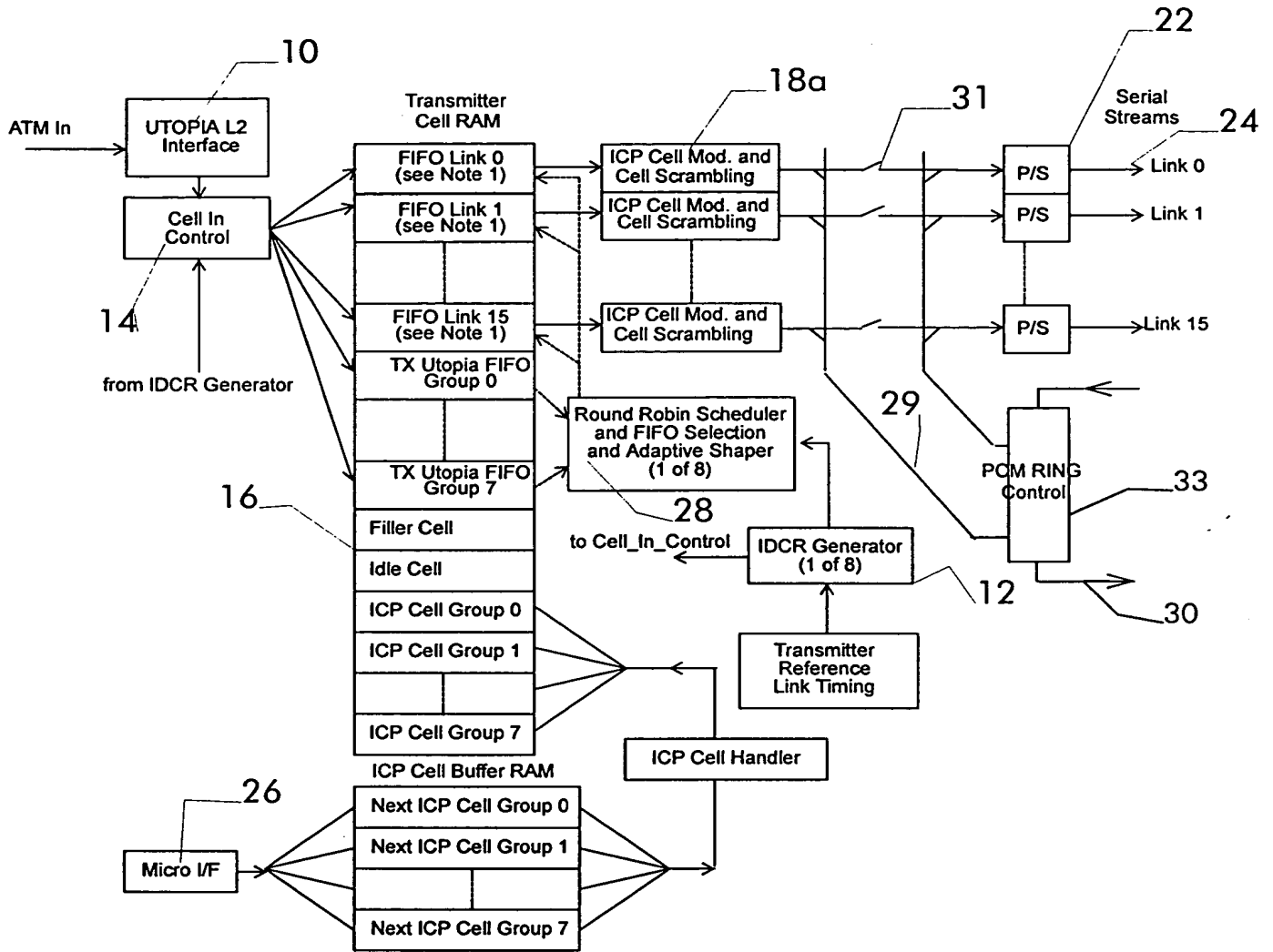


Figure 1

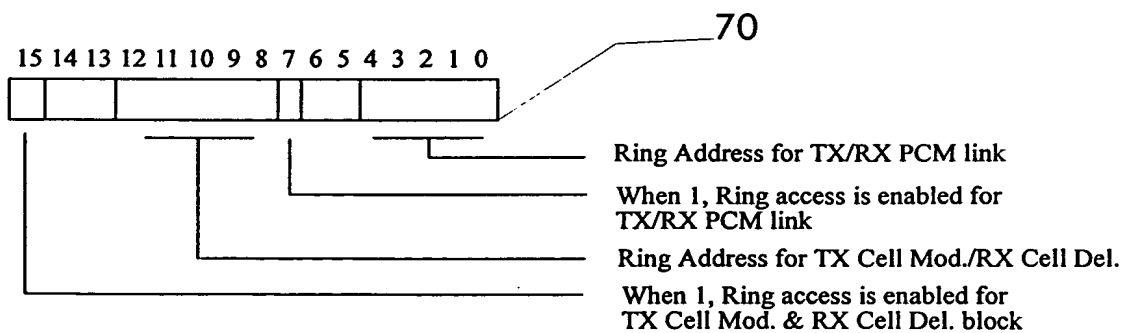


Figure 3

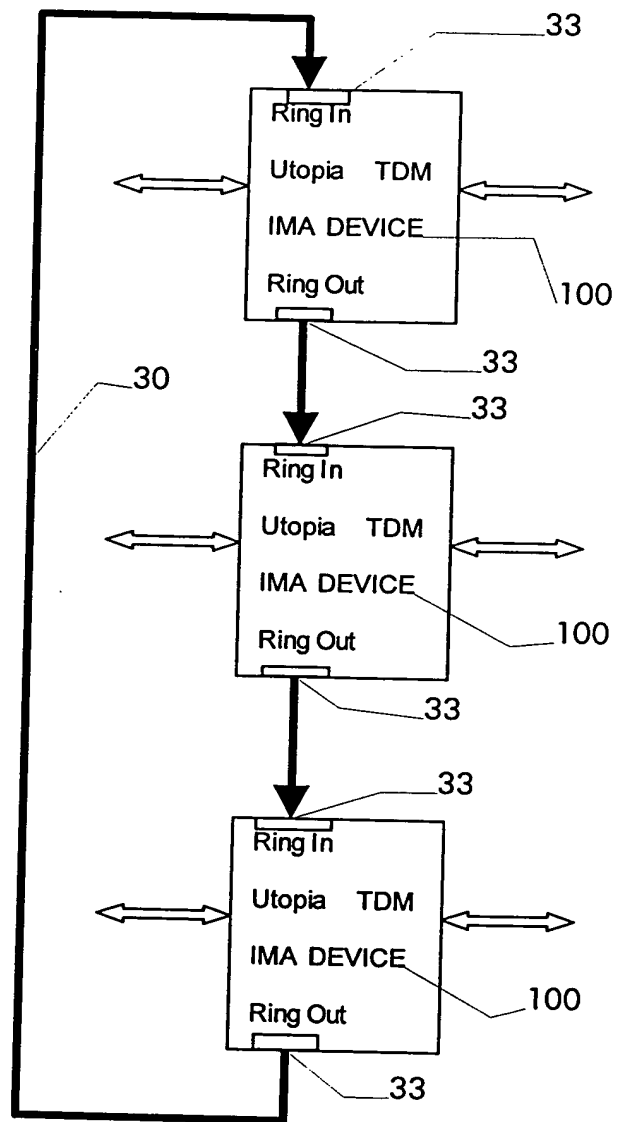


Figure 4

